Intel® 31154 133MHz PCI Bridge Design-In Considerations with IBM PCI-X to PCI-X Bridge

Application Note

August 2003

Order Number: 278806-002

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Revision History

Date	Revision	Description
May 2003	001	This is the first release of this product.
August 2003	002	New document title

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1.0 Objective

This document describes both hardware and software issues that should be considered when migrating from the IBM (r) PCI-X to PCI-X Bridge to the Intel (r) 31154 133MHz PCI Bridge (also called 31154 Bridge).

There are essentially three scenarios here:

- The first is a look at minimal transitional requirements to consider the 31154 Bridge as a socket comparable device with IBM (not taking full advantage of the 31154 Bridge's added features).
- The second is a design that utilizes the IBM but also has designed in the 31154 Bridge's added features.
- The last one involves a pure 31154 Bridge design guide which is not the intention of this application note.

Note: The first two scenarios will be considered. One scenario builds upon the other.

As with any design change, customers should perform thorough validation of their application hardware and software prior to production.

2.0 Socket Comparable Summary

Table 1 summarizes the differences between PCI-X Bridges.

Table 1. PCI-X Bridges Comparison

Function	IBM	Intel
Footprint	304 pin BGA	421 pin BGA (internal superset of IBM)
Core Voltage	2.5V	1.3V
Secondary Clocks	None - - - - P_DRV_MODE Reserved2 P_CFG_BUSY BAR_EN	S_BRGCLKO S_CLKO[8:0] S_CKLI S_CLKSTABLE S_GCLKOE S_CLKOE_2 S_CLKOE_1 S_CLKOE_0 S_CLKOE_3
Buffer Flash Mechanism	None (XCLK_OUT)	QE pin NT_MASK#
Hot Swap Pins	None	HS_ENUM# HS_LSTAT HS_LED_OUT HS_SM HS_FREQ[1:0]
SROM Interface	None	SR_CLK SR_DI SR_DO SR_CS
GPIO	None	GPI0[7:0]
M66EN	None	P_M66EN S_M66EN
Secondary MTT	None	Control Register
RSS Support	None	S_TRISTATE ARB_LOCK
JTAG	Internal test modes	Different test modes
S_PCIXCAP	2 pins	1 pin (no S_PCIXCAP_PU)
REQ/GNT [9:7]	None	S_REG[9:7] S_GNT[9:7]

2.1 Minimal Transitional Requirements

2.1.1 Footprint

The IBM PCI-X Bridge is a 304 pin BGA package. The 31154 Bridge is designed to be socket comparable with the IBM's 304 pin but includes an inner superset of pins for the added features. The total number of pins for the 31154 Bridge is 421 pins in the same 31 mm x 31 mm BGA package.

2.1.2 Voltage Planes

The core voltage (Vdd) for the IBM bridge is 2.5 volts and for the 31154 Bridge its 1.3 volts. The core voltage pins should be tied to the voltage source of VDD (2.5 volts for IBM and 1.3 volts for the 31154 Bridge) These pins map to all the VDD pins (D9, D11,D13,D15, J4, J20, L4, L20,N4,N20, R4, R20, Y9, Y11, Y13, Y15) in the IBM footprint in addition to this we add the following pins to this voltage plane: F6, F8, F10, F15, F17,G18, H6,H19, K6, R6,T18, T19,U6, V7, V9, V14, V18, W13.

VDD2 pins (3.3 volts in IBM) are pin for pin compatible with the following exceptions:

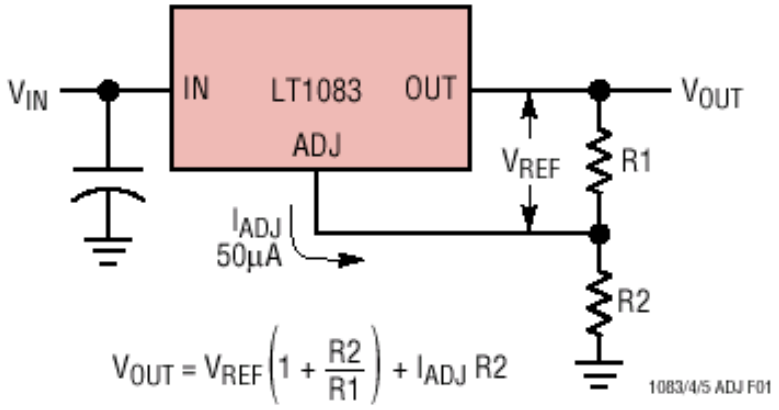
- Pins T1 and H23 are used as P_VIO and S_VIO pins on the 31154 Bridge. Having these tied to VDD would still allow the 31154 Bridge to function properly. (Having the means to isolate PVIO and SVIO later would allow for 5 volt VIO compatibility with legacy PCI devices migrating to PCI-X)
- R-REF pin E5 is for process compensation and could be brought to a pull down resister pad. E5 is not used in the IBM PCI-X Bridge.

The grounds are pin for pin the same with the following additions:

E6, E10, E14,E18, F5,F7,F9, F14,F16,F18-19, G6,G19, H18, J6, K5, K10-14, L10-14, M10-14, N10-14, P5, P6, P10-14, T6, U18, V5-6,V8,V10,V19, W6-12, W14,W19.

If designing for "31154-Ready" with the IBM Bridge, a variable voltage regulator could be used to accommodate the differing VDD requirements using an LT1085 positive adjustable voltage regulator like in the reference design:

Figure 1. LT1085 Positive Adjustable Voltage Regulator



From the LT1083/4/5 data sheet application:

Changing the resistor values is all that is needed to change the voltage from 2.5V to 1.3V.

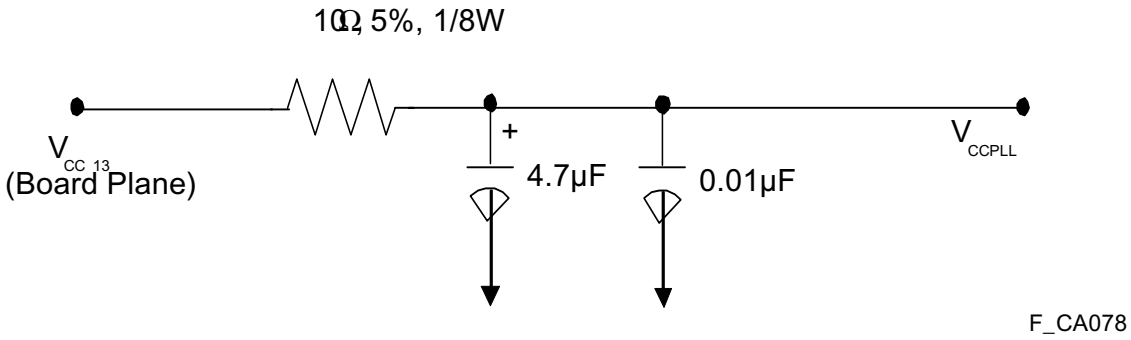
For instance, the following probable resistor value combinations are possible:

For IBM R1=R2=121 ohms 1% precision resistors.

For the 31154 Bridge R1 = 140 ohms R2= 7 ohms 1% precision resistors.

The Analog PLL voltages P_VDDA and S_VDDA (pins A21 and AB21) map to analog PLL voltage pins on the 31154 Bridge as well called P_VCCA and S_VCCA. The following low pass filter circuit provides the recommended isolation for both the IBM and 31154 Bridges:

Figure 2. VCCPLL Lowpass Filter



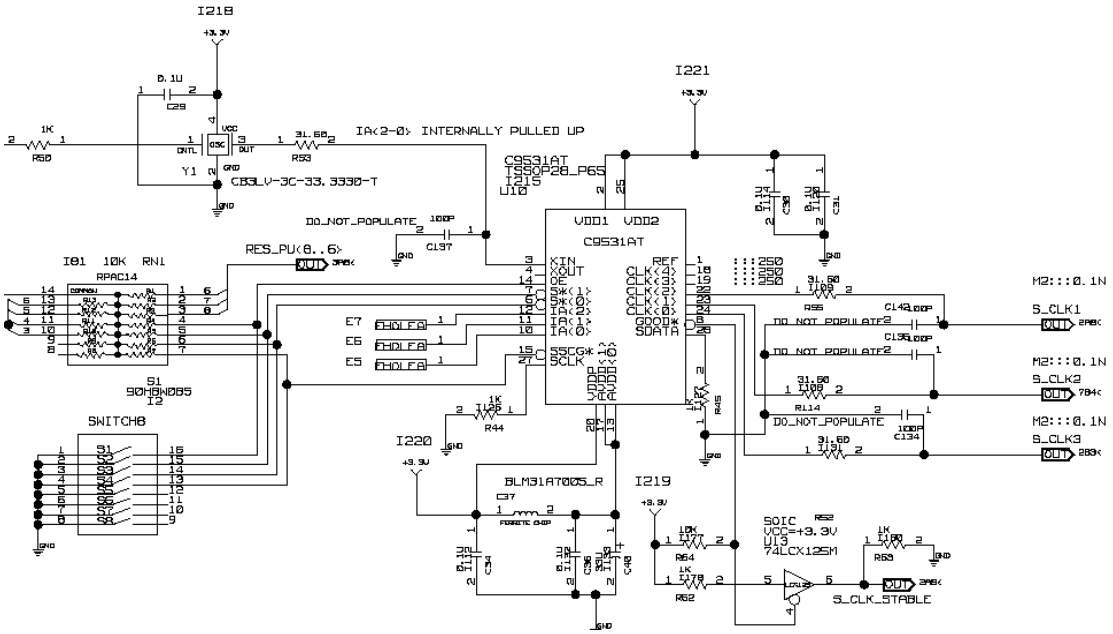
2.1.3 Secondary Clocks

2.1.3.1 IBM Bridge Clock

The IBM Bridge relies on an external clock to provide clocks for devices on the secondary bus.

The suggested design reference uses the following circuitry:

Figure 3. Clock Circuitry



A C9531 clock repeater is used in the IBM reference design to provide the secondary clocks. S_CLK_STABLE feeds back to the IBM device at pin W3 and S_CLK1 feeds into pin AB23 of the IBM bridge's S_CLK.

2.1.3.2 31154 Bridge Clock

The S_CLK_STABLE signal can be brought into the same pin at W3 as well as S_CKL1 can be routed to S_CLKI (pin AB23).

Additional considerations for the associated clocking pins in the 31154 Bridge superset of pins:

— Tie the S_GCLKOE (Global secondary clock disable pin U19) low to tri-state the internal secondary clocks.

— If operating either the primary or secondary bus in conventional PCI mode, the P_M66EN and S_M66EN pins have to be tied high for 66 MHz operation or Low for 33 MHz operation. Bringing these signals out to a pullup as a default, even if the intended operation is PCI-X, should be considered. (S_PCIXCAP will be discussed later)

2.1.4 Buffer Flush Mechanism

The Buffer flushing capability of the 31154 Bridge can be disabled by using a Pull-up resistor for the NT_MASK# signal (New transaction mask pin E15 for IBM mode do not install the resistor). The QE# (queues empty pin D3) signal becomes invalid. For the IBM bridge, Pin D3 is the XCLK_OUT, which is used to monitor the PLL output. IBM suggests having this signal pulled lowed because under normal operations it is in high impedance. With NT_MASK# disabling the QE# status, a pull down will have no impact on the 31154 Bridge.

2.1.5 Compact PCI Hot Swap Pins

The 31154 Bridge adds six pins for Hot swap capability. To disable these under a minimal IBM implementation, the following pins have to be strapped accordingly:

Table 2. Hot Swap Pins

Signal Name	Pin	Setting
HS_ENUM# HS_LSTAT HS_LED_OUT HS_SM HS_FREQ [1:0]	E9 E8 E7 G5 E13. E12	NC Pull-Down NC Pull-down (disables) Pull-down

2.1.6 SROM Interface

The 31154 Bridge adds four pins for the SROM interface. To de-feature SROM, set all signals as follows:

Table 3. SROM Settings

Signal Name	Pin	Setting
SR_CLK SR_DI SR_DO SR_CS	J5 N5 M5 L5	NC NC Pull-up NC

2.1.7 GPIO

The 31154 Bridge makes use of 8 GPIO pins, GPIO [7::0] pins E (16,17,19), V (15,16), W (16,17,18) and can all be brought out to a pad and brought to pull up resistors.

2.1.8 JTAG

The 31154 Bridge employs the same pin for pin functionality as IBM's JTAG interface with the exception of the internal test modes (TMODE [2::0]) but the identical initialization strapping options will function the same. JTAG Comparison

Signal group	31154 Bridge	IBM	Usage
JTAG signal	TDI TDO TMS TCLK TRST#	JTG_TDI JTG_TDO JTG_TMS JTG_TCK JTG_TRST#	same (data in) same (data out) same (test mode select) same (clock) same (reset must be low at P_RST)
Internal test mode	SCAN_ENA TMODE3 TMODE [2::1] TMODE0	T_MODECTL TEST_CEO T_DI [2:1]# T_RI#	Both pull-dn at (31154 Bridge uses to enable test scan) Both pull-dn (both function as a test mode enable) Both pull-up (Internal function)

2.1.9 Secondary PCIXCAP

The IBM PCI-X Bridge uses the programmable pull-up and binary input buffer method for determine the speed of the secondary bus segment. This requires S_PCIXCAP_PU (pin AA1) pin to have a 1K resistor. To operate in 31154 Bridge mode, do not install the 1K resistor.

The 31154 Bridge uses a 3-level comparator method and doesn't use the S_PCIXCAP_PU pin and has this as an unused pin on AA1. S_PCIXCAP becomes a no connect (nc) in the 31154 Bridge.

The signal S_PCIXCAP (R23) has the same functionality as in the IBM Bridge.

2.1.10 Secondary Arbiters

The IBM Bridge allocates six secondary Req/Gnt pairs for arbitration. S_REQ1GNT# and S_GNT1REQ# dual function pins are the same as the 31154 Bridge S_REQ[0]#/BR_GNT# and S_GNT[0]#/BR_GNT# pins. Table 4 includes a summary of the similarities and differences of these pins.

Table 4. Arbiter Pins

IBM	31154 Bridge	Pin(s)	Note
S_REQ1GNT#	S_REQ	AA23	
S_GNT1REQ#	[0]#/BR_GNT#	AA19	
S_REQ [6::2]#	S_GNT	AC3,AB5,AB3	31154 Bridge 0 to 5
-	[0]#/BR_GNT#	W2, AA2	(IBM 1 to 6)
S_GNT[6::2]#	-	AC4,AB4,AC5	
-	S_REQ [5::1]#	Y2, AB1	
N/A	-	W15,T5, W5	Pull-up
N/A	S_GNT [5::1]#	V17, R5, U5	NC
	S_REQ [8::6] #		
	S_GNT [8::6]#		

2.2 Maximizing an Existing IBM Design for Full 31154 Bridge Benefits:

If a design is taking place to incorporate the IBM 133 PCI-x Bridge because of its availability but the design would like to take advantage of the added features and benefits of the 31154 Bridge when it does become available, then the following features have to be considered in addition to the Minimal transitions in the previous section:

- GPIO
- Adding SROM capability
- Additional routing for secondary Clocks provided by the 31154 Bridge.
- Making use of the cPCI HS pins
- Redundant System Slot /cPCI specific (S_TRISATE, ARB_LOCK, QE and NT_MASK)
- Opaque memory, Private Device masking and IDSEL selections

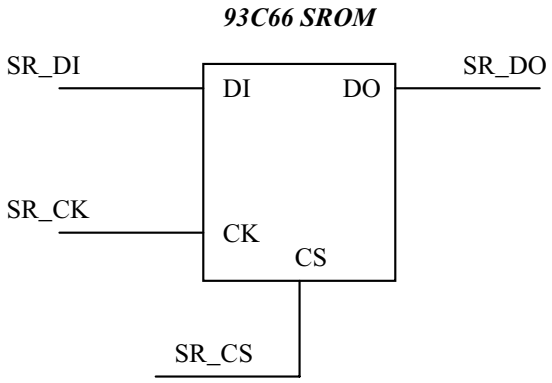
2.2.1 GPIO Interface

The 31154 Bridge makes use of 8 GPIO pins, GPIO [7::0] pins E (16,17,19), V (15,16), W (16,17,18) and can all be routed out to external logic or connector. These should be brought to pull up resistors if unused.

2.2.2 Adding SROM Capabilities:

The 31154 Bridge has a microwire SROM interface to provide for configuration preloading during initializations. The four associated pins could be brought out to the footprint of a 93C66 device as follows:

Figure 4. SROM Connections



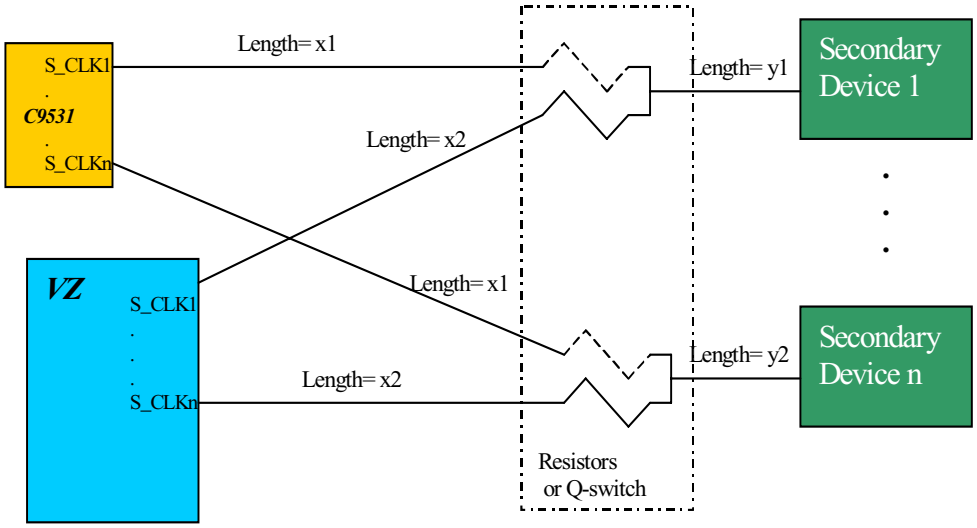
Populate the SROM when the 31154 Bridge is in place.

2.2.3 Additional Routing Suggestions for the Secondary Clocks

Keep in mind here that ultimately the best clock scheme is a direct point-to-point connection. If you are designing to take advantage of the 31154 Bridge's ability to provide additional clocks with no added circuitry while still having the hooks in place for the IBM bridge because of availability, there are risks to be considered. If it is advantageous to wait for the 31154 Bridge's availability then design accordingly without any considerations for the IBM. Otherwise, extreme care in matching switched routing lengths must be maintained at all times.

Depending on the number of loads on the secondary, a switching scheme could facilitate both scenarios. Route the clocks of the secondary loads of equal length to a pair of zero-ohm resistor pads or a three terminal high impedance quick switch and run the two sets of clocks at equal lengths to the resistors (see Figure 5).

Figure 5. Clock Routing Considerations



To operate in IBM mode, populate the top set of resistors or enable that bank of q-switches. The overall routing lengths x1+y1 must be equal to x2 + y2 within a +/- 10 mil tolerance.

2.2.4 Hotswap Ready and Redundant System Slot (RSS) Support for cPCI

The 31154 Bridge is a hotswap ready device. If the future system is intended for a Hotswap application, signals in Table 5 can be brought out to the appropriate circuitry.

Table 5. Hotswap Signals

Signal	Pin	Type	Function
HS_ENUM#	E9	Output	To ENUM# Signal on cPCI connector
HS_LSTAT	E8	Input	To Ejector Handle Switch
HS_LED_OUT	E7	Input	To LED
HS_SM	G5	Input	Pull-down (disables) if no SROM preload is used
HS_FREQ [1:0]	E13, E12	Input	Both Pulled down if primary is in a Conventional PCI otherwise Pull-dn/up according to intended Pri- bus freq. during a Hotswap event as follows: 01 for PCI-X 66 MHz 10 for PCI-X 100 MHz 11 for PCI-X 133 MHz
S_TRISTATE	E11	Input	Pull-down in non-RSS applications To Assert, set to a "1" when system wants to tri-state the secondary bus outputs using external logic.
S_ARB_DISABLE / S_ARB_LOCK	T21	Input	Pull-down to enable internal arbiter, pin MUST have either a pull-down or pull-up resistor and cannot float.

2.2.5 Buffer Flush Management Capabilities

The 31154 Bridge adds buffer management control that can be accessed by external logic. A QE# pin (D3- Formerly IBM's XCLKOUT) to deliver a "queue-empty" status to external logic. In IBM designs, this signal goes to a pull down. If the added circuitry to monitor this signal is planned in a future design, then the pull-down resistor can be depopulated. The QE# signal could be routed to an input of additional logic (FPGA or PAL) that will be populated when the design is built with the 31154 Bridge.

The buffer management logic may also want to incorporate the NT_MASK# pin (E15) to tell the 31154 Bridge not to enqueue any new transactions (except configuration transactions). Used with the above pin the additional logic could flush the 31154 Bridge request and data queues. The buffer flush feature is used to complete transactions in mid flight at the time of a CPU fail-over operation, a key element to the cPCI Redundant System Slot fail-over process.

2.2.6 Opaque Memory Operations

The 31154 Bridge uses the same mechanism and pins to enable an opaque memory mode for devices on the secondary side of the bridge. OPAQUE_EN pin AA18 and IDSEL_MASK pin AC22 map to IBM's OPAQUE_EN and IDSEL_REROUTE pins respectively. The 31154 Bridge

allows for a device who's IDSEL is attached to S_AD<21::16> to be hidden when in private device mode. In the IBM bridge, these are slightly different from S_AD<29>, S_AD<25>, S_AD<23::20> and S_AD<17>.

The default hidden memory range varies as well. In the 31154 Bridge, the top of the half the entire 18 Exa-Byte range of memory space window is selected while the IBM bridge defaults the top 4 GB range. The default can be changed in configuration and allow any range including the entire addressable memory window.

Table 6 briefly defines these differences:

Table 6. Opaque Memory Comparison

Signal	How Used in the 31154 Bridge	How Used in IBM Bridge
IDSEL_MASK (IDSEL_REROUTE)	Devices on S_AD<21::16>hidden.	S_AD<29,25,23-20,17> hidden
OPAQUE_EN	Top half of the 264 addressable memory window	Top 4GB window

3.0 Significant Register Differences

This section provides details on the high level differences found between the two bridge devices. The specific focus of this section is on the fundamental changes in the standard PCI configuration header and those device-specific registers that pertain to the added features discussed in the previous sections of this document.

Note: This document does not provide detail on the description of registers or details of each device specific register mapping.

3.1 Standard PCI Configuration Registers

The 31154 Bridge does not support BAR_EN (pin G2 of the IBM bridge... this is S_CLKOEN2 in the 31154 Bridge) function like the IBM bridge. The IBM bridge support a Base Address Register 0 and Base Address Register 1 at offsets x10 and x14 whenever BAR_EN was strapped low. IBM also makes reference to an Expansion ROM BAR at offset x38. All of these are reserved in the 31154 Bridge.

The following table identifies these fundamental differences:

Table 7. PCI Configuration Comparison

Offset	31154 Bridge	IBM Reg Name
x10	Reserved	Lower Base Address Reg 0
x14	Reserved	Upper Base Address Reg 1
x38	Reserved	Expansion ROM Base Addresses

3.2 Device Specific Registers

This section describes Device Specific Registers that are associated with the following added features of the 31154 Bridge:

- Opaque Memory Registers
- SROM
- GPIO
- Multi Transaction Timer (MTT)
- 31154 Bridge Control Registers

This section only serves as a means of identifying some of the fundamental differences in the 31154 Bridge configuration register set and does not go into any great detail on what the specific settings should be. Please refer to the 31154 Bridge Data sheet for additional information.

3.2.1 Opaque Memory Registers

To facilitate opaque memory operation in the 31154 Bridge, there are four registers associated with this feature as opposed to the five in the IBM:

- Opaque Memory Enable (Offset 46h in 31154 Control Register Bit 11)
- OMBL:Opaque Memory Base and Limit Register (Offset 6Ch)
- OMBU32: Opaque Memory Base Upper 32 bits (Offset 6Ch)
- OMLU32: Opaque Memory Limit Upper 32 bits (Offset 70h)

Default is to have the upper half of the 264 addressable range as Opaque Memory.

3.2.2 SROM Registers and Those Affected Serial Preload

The following two registers are associated with SROM:

- SR_ADDR: Serial ROM Address Register (Offset 4Ah)
- SR_DATA: Serial ROM Data Register (Offset 4Ch)

The serial ROM preload is capable of writing values into most of the registers in the device specific region of the 31154 Bridge's configuration space (Offsets 40h -74h). The exceptions are those associated with status reporting (GPIO, MISC, VZ).

The following registers in the 31154 Bridge's PCI Extended Capabilities List region of configuration space (offsets D4h-FCh) can be written to during an SROM preload:

- SLT_NUM: Slot Number Register (offset D6h)
- CS_NUM: Chassis Number Register (offset D8h)
- PM_NXTP: Power Management Next Pointer Register (offset DDh)
- PM_C: Power Management Capabilities (offset DEh)
- PX_NXTP: PCI-X Next Item Pointer (offset F1h)

3.2.3 GPIO Registers

The following three registers are associated with the GPIO ports:

- GPIO_PINCFG: GPIO Pin Configuration Register (Offset 68h)
- GPIO_W1TT_DATA: GPIO "Write 1 to Toggle" Output Data (offset 69h)
- GPIO_PINSTAT: GPIO Pin Status Register (offset 6Ah)

3.2.4 Multi-Transaction Timer (MTT) Register

The 31154 Bridge employs the MTT to allow better IO bus utilization with multiple agents. It provides a better level of concurrency for agents that issue address fragmented traffic (smaller bursts) against larger burst traffic agents. The MTT register can be used to set the number of clocks that a secondary bus master may have its grant asserted. The Offset is at 50h.

3.2.5 31154 Bridge Control Registers

The 31154 Bridge has three control registers:

- VCR0: 31154 Bridge Control Register 0 (offset 43h)
- VCR1: 31154 Bridge Control Register 1 (offset 44h)
- VCR2: 31154 Bridge Control Register 2 (offset 46h)

VCR0 is used for buffer flush management and queue control.

VCR1 is used for timer controls (primary and secondary discard timers, Watch dog timers, command alias mapping).

VCR2 is used for Opaque memory enable and secondary clock outputs control.

4.0 Pins Not Used by the 31154 Bridge but Needed for the IBM PCI-X Bridge

Some signals in the IBM PCI-X bridge are not needed in the 31154 Bridge. Table 8 summarizes these variances:

Table 8. Pins Not Used

IBM Signal	Pin	Type	Handled in the 31154 Bridge
S_PCIXCAP_PU	AA1	Input	No connect
XCLK_OUT	D3	Output	Becomes QE status
P_DRV_MODE	E2	Input	Becomes S_CLKOEN<2>
S_DRV_MODE	AC7	Input	Reserved pin
VDD2	T1	Power	Becomes S_VIO
VDD2	H23	Power	Becomes P_VIO

Appendix A Ballout of the 31154 Bridge with Pin Differences Highlighted

Figure 6. Ballout with Pin Differences (Left side of map)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	P_ ACK64#	P_ AD56	P_ AD60	P_ CBE4#	VSS	P_ CBE7#	VCCP	P_ PAR64	VSS	VSS	VCCP
B	P_ AD43	VSS	P_ AD54	P_ SERR#	P_ AD49	P_ AD50	P_ AD52	P_ AD55	P_ AD57	P_ AD59	P_ AD63	P_ CBE6#
C	SCAN_ EN	P_ AD48	VSS	P_ STOP#	VCCP	S_CLK OEN3	P_ AD53	P_ PERR#	P_ AD58	P_ AD61	P_ CBE5#	P_ REQ64#
D	S_CLK OEN2	P_ AD47	QE	VSS	VCCP	P_ AD51	VCCP	VSS	VCC	P_ AD62	VCC	VSS
E	P_ AD38	S_CLK OEN1	P_ AD45	VCCP	R_REF	VSS	HS_ LED_ OUT	HS_ LSTAT	HS_ ENUM#	VSS	S_TRI STATE	HS_ FREQ0
F	VSS	P_ AD42	P_ AD44	P_ AD46	VSS	VCC	VSS	VCC	VSS	VCC		
G	P_ AD36	S_CLK OEN0	P_ AD41	VCCP	HS_ SM	VSS						
H	P_ AD35	P_ AD39	P_ AD40	VSS	P_ M66EN	VCC						
J	P_ AD33	P_ AD34	P_ AD37	VCC	SR_ CLK	VSS						
K	VSS	S_ AD34	S_ AD33	S_ AD32	VSS	VCC				VSS	VSS	VSS
L	P_ AD32	S_ AD36	S_ AD35	VCC	SR_CS					VSS	VSS	VSS
M	VCCP	S_ AD39	S_ AD38	VSS	SR_DO					VSS	VSS	VSS
N	VSS	S_ AD41	S_ AD40	VCC	SR_DI					VSS	VSS	VSS
P	VSS	S_ AD47	S_ AD45	S_ AD43	VSS	VSS				VSS	VSS	VSS
R	S_ AD37	S_ AD49	S_ AD48	VCC	S_ GNT7#	VCC						
T	S_VIO	S_ AD51	S_ AD50	VSS	S_ REQ7#	VSS						
U	S_ AD42	S_ AD53	S_ AD52	VCCP	S_ GNT6#	VCC						
V	VSS	S_ AD55	S_MAX 100	S_ AD54	VSS	VSS	VCC	VSS	VCC	VSS		
W	S_ AD44	S_ REQ2#	S_CLK STABLE	VCCP	S_ REQ6#	VSS	VSS	VSS	VSS	VSS	VSS	VSS
Y	S_ AD46	S_ GNT2#	S_ AD56	VSS	VCCP	S_ AD57	VCCP	VSS	VCC	S_ CBE7#	VCC	VSS
AA	NC	S_ REQ1#	VSS	TMODE 2	S_ AD58	S_ AD59	S_ AD61	S_ ACK64#	S_ AD00	S_ PAR64	S_ CBE5#	S_ AD06
AB	S_ GNT1#	VSS	S_ REQ3#	S_ GNT4#	S_ REQ4#	S_ AD60	S_ AD62	S_ AD63	S_ AD01	S_ CBE6#	S_ AD04	S_ CBE0#
AC	VSS	VCCP	S_ REQ5#	S_ GNT5#	S_ GNT3#	VSS	RSRV1	S_ CBE4#	S_ AD02	VSS	S_ AD03	VCCP
	1	2	3	4	5	6	7	8	9	10	11	12

B2238-01

Figure 7. Ballout with Pin Differences (Right side of map)

13	14	15	16	17	18	19	20	21	22	23	
P_CBE0#	VSS	P_CBE3#	P_IRDY#	P_FRAME	VSS	P_AD04	P_AD07	P_VCCA	VCCP	VSS	A
P_AD00	P_AD02	P_TRDY#	P_AD05	P_AD08	P_CBE1#	P_IDSEL	P_AD15	P_REQ#	VSS	TDO	B
P_AD01	MT0#	P_AD03	P_AD06	P_AD09	P_PAR	P_AD10	P_GNT#	VSS	TDI	TRST#	C
VCC	P_CBE2#	VCC	VSS	VCCP	P_AD11	VCCP	VSS	P_DEVSEL#	TMS	P_AD22	D
HS_FREQ1	VSS	HT_MASK#	P_GPIO0	P_GPIO1	VSS	P_GPIO2	VCCP	P_CLK	P_RST#	P_AD24	E
	VSS	VCC	VSS	VCC	VSS	VSS	P_AD13	TCK	P_AD12	VSS	F
					VCC	VSS	VCCP	P_AD16	P_AD14	P_AD26	G
					VSS	VCC	VSS	P_AD18	P_AD17	P_VIO	H
					P_CLKO0	P_CLKO2	VCC	P_AD20	P_AD19	P_AD31	J
VSS	VSS				P_CLKO1	P_CLKO4	P_AD25	P_AD23	P_AD21	VSS	K
VSS	VSS					P_CLKO3	VCC	P_AD28	P_AD27	VSS	L
VSS	VSS					P_CLKO5	VSS	P_AD30	P_AD29	S_AD27	M
VSS	VSS					P_CLKO6	VCC	S_AD30	S_AD31	S_AD25	N
VSS	VSS				S_BRGCLKO	S_CLK07	S_AD26	S_AD28	S_AD29	VSS	P
					S_M66EN	S_CLKO8	VCC	S_AD22	S_AD24	S_PCIXCAP	R
					VCC	VCC	VSS	S_ARB_DISABLE	S_AD20	S_AD23	T
					VSS	S_GCLKOEN	VCCP	S_AD18	S_AD19	S_RST#	U
	VCC	GPIO3	GPIO5	S_GNT8#	VCC	VSS	S_AD14	S_AD16	S_AD17	VSS	V
VCC	VSS	S_REQ8#	GPIO4	GPIO6	GPIO7	VSS	VCCP	S_AD15	TMODE0	S_AD21	W
VCC	S_TRDY#	VCC	VSS	VCCP	S_AD11	VCCP	VSS	TMODE1	DEV_64BIT#	TMODE3	Y
S_AD07	S_FRAME#	S_CBE3#	S_AD10	S_PAR	OPAQUE_EN	S_GNT0#	S_AD13	VSS	RSTV0	S_REQ0#	AA
S_REQ64#	S_CBE2#	S_AD09	S_CBE1#	S_PERR#	S_AD12	S_SERR#	S_STOP#	S_VCCA	VSS	S_CLKI	AB
VSS	VSS	S_AD05	VCCP	S_AD08	VSS	S_IRDY#	MT1#	S_DEVSEL#	IDSEL_MASK	VSS	AC
13	14	15	16	17	18	19	20	21	22	23	

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Appendix B Complete Side by Side Signal Listing to Grid Mapping

Table 9. Complete Side by Side Signal Listing

IBM		31154		Name Same?
AC22	IDSEL_REROUTE_EN	AC22	IDSEL_MASK	Some Functional Difference
AA1	S_PCIXCAP_PU	AA1	NC	OK
D3	XCLK_OUT	D3	QE	OK
AA22	S_IDSEL	AA22	RSRV0	No secondary config access
AC7	S_DRVR_MODE	AC7	RSRV1	Not needed for our drivers
G2	BAR_EN	G2	S_CLKOEN0	No support for BAR_EN
E2	P_DRVR_MODE	E2	S_CLKOEN1	Not needed for our drivers
D1	RESERVED2	D1	S_CLKOEN2	OK
C6	P_CFG_BUSY	C6	S_CLKOEN3	Not functional in IBM part due to errata
C1	T_MODECTL	C1	SCAN_EN	OK - Test Mode
W22	T_RI	W22	TMODE0	OK - Test Mode
Y21	T_DI1	Y21	TMODE1	OK - Test Mode
AA4	T_DI2	AA4	TMODE2	OK - Test Mode
Y23	TEST_CE0	Y23	TMODE3	OK - Test Mode
E16		E16	GPIO0	new pin
E17		E17	GPIO1	new pin
E19		E19	GPIO2	new pin
V15		V15	GPIO3	new pin
W16		W16	GPIO4	new pin
V16		V16	GPIO5	new pin
W17		W17	GPIO6	new pin
W18		W18	GPIO7	new pin
E9		E9	HS_ENUM#	new pin
E12		E12	HS_FREQ0	new pin
E13		E13	HS_FREQ1	new pin
E7		E7	HS_LED_OUT	new pin
E8		E8	HS_LSTAT	new pin
G5		G5	HS_SM	new pin
E15		E15	NT_MASK#	new pin
H5		H5	P_M66EN	new pin
E5		E5	R_REF	new pin
P18		P18	S_BRGCLKO	new pin
J18		J18	S_CLKO0	new pin
K18		K18	S_CLKO1	new pin
J19		J19	S_CLKO2	new pin
L19		L19	S_CLKO3	new pin
K19		K19	S_CLKO4	new pin
M19		M19	S_CLKO5	new pin
N19		N19	S_CLKO6	new pin
P19		P19	S_CLKO7	new pin

R19	R19	S_CLKO8	new pin
U19	U19	S_GCLKOEN	new pin
U5	U5	S_GNT6#	new pin
R5	R5	S_GNT7#	new pin
V17	V17	S_GNT8#	new pin
R18	R18	S_M66EN	new pin
W5	W5	S_REQ6#	new pin
T5	T5	S_REQ7#	new pin
W15	W15	S_REQ8#	new pin
E11	E11	S_TRISTATE	new pin
J5	J5	SR_CLK	new pin
L5	L5	SR_CS	new pin
N5	N5	SR_DI	new pin
M5	M5	SR_DO	new pin
F10	F10	VCC	new pin
F15	F15	VCC	new pin
F17	F17	VCC	new pin
F6	F6	VCC	new pin
F8	F8	VCC	new pin
G18	G18	VCC	new pin
H19	H19	VCC	new pin
H6	H6	VCC	new pin
K6	K6	VCC	new pin
R6	R6	VCC	new pin
T18	T18	VCC	new pin
T19	T19	VCC	new pin
U6	U6	VCC	new pin
V14	V14	VCC	new pin
V18	V18	VCC	new pin
V7	V7	VCC	new pin
V9	V9	VCC	new pin
W13	W13	VCC	new pin
E10	E10	VSS	new pin
E14	E14	VSS	new pin
E18	E18	VSS	new pin
E6	E6	VSS	new pin
F14	F14	VSS	new pin
F16	F16	VSS	new pin
F18	F18	VSS	new pin
F19	F19	VSS	new pin
F5	F5	VSS	new pin
F7	F7	VSS	new pin
F9	F9	VSS	new pin
G19	G19	VSS	new pin
G6	G6	VSS	new pin
H18	H18	VSS	new pin
J6	J6	VSS	new pin

K10		K10	VSS	new pin
K11		K11	VSS	new pin
K12		K12	VSS	new pin
K13		K13	VSS	new pin
K14		K14	VSS	new pin
K5		K5	VSS	new pin
L10		L10	VSS	new pin
L11		L11	VSS	new pin
L12		L12	VSS	new pin
L13		L13	VSS	new pin
L14		L14	VSS	new pin
M10		M10	VSS	new pin
M11		M11	VSS	new pin
M12		M12	VSS	new pin
M13		M13	VSS	new pin
M14		M14	VSS	new pin
N10		N10	VSS	new pin
N11		N11	VSS	new pin
N12		N12	VSS	new pin
N13		N13	VSS	new pin
N14		N14	VSS	new pin
P10		P10	VSS	new pin
P11		P11	VSS	new pin
P12		P12	VSS	new pin
P13		P13	VSS	new pin
P14		P14	VSS	new pin
P5		P5	VSS	new pin
P6		P6	VSS	new pin
T6		T6	VSS	new pin
U18		U18	VSS	new pin
V10		V10	VSS	new pin
V19		V19	VSS	new pin
V5		V5	VSS	new pin
V6		V6	VSS	new pin
V8		V8	VSS	new pin
W10		W10	VSS	new pin
W11		W11	VSS	new pin
W12		W12	VSS	new pin
W14		W14	VSS	new pin
W19		W19	VSS	new pin
W6		W6	VSS	new pin
W7		W7	VSS	new pin
W8		W8	VSS	new pin
W9		W9	VSS	new pin
Y22	64_BIT_DEVICE#	Y22	DEV_64BIT#	
AA18	OPAQUE_EN	AA18	OPAQUE_EN	
A2	P_ACK64#	A2	P_ACK64#	

B13	P_AD(00)	B13	P_AD00		
C13	P_AD(01)	C13	P_AD01		
B14	P_AD(02)	B14	P_AD02		
C15	P_AD(03)	C15	P_AD03		
A19	P_AD(04)	A19	P_AD04		
B16	P_AD(05)	B16	P_AD05		
C16	P_AD(06)	C16	P_AD06		
A20	P_AD(07)	A20	P_AD07		
B17	P_AD(08)	B17	P_AD08		
C17	P_AD(09)	C17	P_AD09		
C19	P_AD(10)	C19	P_AD10		
D18	P_AD(11)	D18	P_AD11		
F22	P_AD(12)	F22	P_AD12		
F20	P_AD(13)	F20	P_AD13		
G22	P_AD(14)	G22	P_AD14		
B20	P_AD(15)	B20	P_AD15		
G21	P_AD(16)	G21	P_AD16		
H22	P_AD(17)	H22	P_AD17		
H21	P_AD(18)	H21	P_AD18		
J22	P_AD(19)	J22	P_AD19		
J21	P_AD(20)	J21	P_AD20		
K22	P_AD(21)	K22	P_AD21		
D23	P_AD(22)	D23	P_AD22		
K21	P_AD(23)	K21	P_AD23		
E23	P_AD(24)	E23	P_AD24		
K20	P_AD(25)	K20	P_AD25		
G23	P_AD(26)	G23	P_AD26		
L22	P_AD(27)	L22	P_AD27		
L21	P_AD(28)	L21	P_AD28		
M22	P_AD(29)	M22	P_AD29		
M21	P_AD(30)	M21	P_AD30		
J23	P_AD(31)	J23	P_AD31		
L1	P_AD(32)	L1	P_AD32		
J1	P_AD(33)	J1	P_AD33		
J2	P_AD(34)	J2	P_AD34		
H1	P_AD(35)	H1	P_AD35		
G1	P_AD(36)	G1	P_AD36		
J3	P_AD(37)	J3	P_AD37		
E1	P_AD(38)	E1	P_AD38		
H2	P_AD(39)	H2	P_AD39		
H3	P_AD(40)	H3	P_AD40		
G3	P_AD(41)	G3	P_AD41		
F2	P_AD(42)	F2	P_AD42		
B1	P_AD(43)	B1	P_AD43		
F3	P_AD(44)	F3	P_AD44		
E3	P_AD(45)	E3	P_AD45		
F4	P_AD(46)	F4	P_AD46		

D2	P_AD(47)	D2	P_AD47		
C2	P_AD(48)	C2	P_AD48		
B5	P_AD(49)	B5	P_AD49		
B6	P_AD(50)	B6	P_AD50		
D6	P_AD(51)	D6	P_AD51		
B7	P_AD(52)	B7	P_AD52		
C7	P_AD(53)	C7	P_AD53		
B3	P_AD(54)	B3	P_AD54		
B8	P_AD(55)	B8	P_AD55		
A3	P_AD(56)	A3	P_AD56		
B9	P_AD(57)	B9	P_AD57		
C9	P_AD(58)	C9	P_AD58		
B10	P_AD(59)	B10	P_AD59		
A4	P_AD(60)	A4	P_AD60		
C10	P_AD(61)	C10	P_AD61		
D10	P_AD(62)	D10	P_AD62		
B11	P_AD(63)	B11	P_AD63		
A13	P_C/BE(0)#	A13	P_CBE0#		
B18	P_C/BE(1)#	B18	P_CBE1#		
D14	P_C/BE(2)#	D14	P_CBE2#		
A15	P_C/BE(3)#	A15	P_CBE3#		
A5	P_C/BE(4)#	A5	P_CBE4#		
C11	P_C/BE(5)#	C11	P_CBE5#		
B12	P_C/BE(6)#	B12	P_CBE6#		
A7	P_C/BE(7)#	A7	P_CBE7#		
E21	P_CLK	E21	P_CLK		
D21	P_DEVSEL#	D21	P_DEVSEL#		
A17	P_FRAME#	A17	P_FRAME#		
C20	P_GNT#	C20	P_GNT#		
B19	P_IDSEL	B19	P_IDSEL		
A16	P_IRDY#	A16	P_IRDY#		
C14	P_LOCK#	C14	MT0#		
C18	P_PAR	C18	P_PAR		
A9	P_PAR64	A9	P_PAR64		
C8	P_PERR#	C8	P_PERR#		
B21	P_REQ#	B21	P_REQ#		
C12	P_REQ64#	C12	P_REQ64#		
E22	P_RST#	E22	P_RST#		
B4	P_SERR#	B4	P_SERR#		
C4	P_STOP#	C4	P_STOP#		
B15	P_TRDY#	B15	P_TRDY#		
A21	P_VDDA	A21	P_VCCA		
H23	VDD2	H23	P_VIO		
AA8	S_ACK64#	AA8	S_ACK64#		
AA9	S_AD(00)	AA9	S_AD00		
AB9	S_AD(01)	AB9	S_AD01		
AC9	S_AD(02)	AC9	S_AD02		

AC11	S_AD(03)	AC11	S_AD03		
AB11	S_AD(04)	AB11	S_AD04		
AC15	S_AD(05)	AC15	S_AD05		
AA12	S_AD(06)	AA12	S_AD06		
AA13	S_AD(07)	AA13	S_AD07		
AC17	S_AD(08)	AC17	S_AD08		
AB15	S_AD(09)	AB15	S_AD09		
AA16	S_AD(10)	AA16	S_AD10		
Y18	S_AD(11)	Y18	S_AD11		
AB18	S_AD(12)	AB18	S_AD12		
AA20	S_AD(13)	AA20	S_AD13		
V20	S_AD(14)	V20	S_AD14		
W21	S_AD(15)	W21	S_AD15		
V21	S_AD(16)	V21	S_AD16		
V22	S_AD(17)	V22	S_AD17		
U21	S_AD(18)	U21	S_AD18		
U22	S_AD(19)	U22	S_AD19		
T22	S_AD(20)	T22	S_AD20		
W23	S_AD(21)	W23	S_AD21		
R21	S_AD(22)	R21	S_AD22		
T23	S_AD(23)	T23	S_AD23		
R22	S_AD(24)	R22	S_AD24		
N23	S_AD(25)	N23	S_AD25		
P20	S_AD(26)	P20	S_AD26		
M23	S_AD(27)	M23	S_AD27		
P21	S_AD(28)	P21	S_AD28		
P22	S_AD(29)	P22	S_AD29		
N21	S_AD(30)	N21	S_AD30		
N22	S_AD(31)	N22	S_AD31		
K4	S_AD(32)	K4	S_AD32		
K3	S_AD(33)	K3	S_AD33		
K2	S_AD(34)	K2	S_AD34		
L3	S_AD(35)	L3	S_AD35		
L2	S_AD(36)	L2	S_AD36		
R1	S_AD(37)	R1	S_AD37		
M3	S_AD(38)	M3	S_AD38		
M2	S_AD(39)	M2	S_AD39		
N3	S_AD(40)	N3	S_AD40		
N2	S_AD(41)	N2	S_AD41		
U1	S_AD(42)	U1	S_AD42		
P4	S_AD(43)	P4	S_AD43		
W1	S_AD(44)	W1	S_AD44		
P3	S_AD(45)	P3	S_AD45		
Y1	S_AD(46)	Y1	S_AD46		
P2	S_AD(47)	P2	S_AD47		
R3	S_AD(48)	R3	S_AD48		
R2	S_AD(49)	R2	S_AD49		

T3	S_AD(50)	T3	S_AD50		
T2	S_AD(51)	T2	S_AD51		
U3	S_AD(52)	U3	S_AD52		
U2	S_AD(53)	U2	S_AD53		
V4	S_AD(54)	V4	S_AD54		
V2	S_AD(55)	V2	S_AD55		
Y3	S_AD(56)	Y3	S_AD56		
Y6	S_AD(57)	Y6	S_AD57		
AA5	S_AD(58)	AA5	S_AD58		
AA6	S_AD(59)	AA6	S_AD59		
AB6	S_AD(60)	AB6	S_AD60		
AA7	S_AD(61)	AA7	S_AD61		
AB7	S_AD(62)	AB7	S_AD62		
AB8	S_AD(63)	AB8	S_AD63		
T21	INT_ARB_EN#	T21	S_ARB_DISABLE		
AB12	S_C/BE(0)#	AB12	S_CBE0#		
AB16	S_C/BE(1)#	AB16	S_CBE1#		
AB14	S_C/BE(2)#	AB14	S_CBE2#		
AA15	S_C/BE(3)#	AA15	S_CBE3#		
AC8	S_C/BE(4)#	AC8	S_CBE4#		
AA11	S_C/BE(5)#	AA11	S_CBE5#		
AB10	S_C/BE(6)#	AB10	S_CBE6#		
Y10	S_C/BE(7)#	Y10	S_CBE7#		
AB23	S_CLK	AB23	S_CLKI		
W3	S_CLK_STABLE	W3	S_CLKSTABLE		
AC21	S_DEVSEL#	AC21	S_DEVSEL#		
AA14	S_FRAME#	AA14	S_FRAME#		
AA19	S_GNT1REQ#	AA19	S_GNT0#		
AB1	S_GNT2#	AB1	S_GNT1#		
Y2	S_GNT3#	Y2	S_GNT2#		
AC5	S_GNT4#	AC5	S_GNT3#		
AB4	S_GNT5#	AB4	S_GNT4#		
AC4	S_GNT6#	AC4	S_GNT5#		
AC19	S_IRDY#	AC19	S_IRDY#		
AC20	S_LOCK#	AC20	MT1#		
V3	S_SEL100	V3	S_MAX100		
AA17	S_PAR	AA17	S_PAR		
AA10	S_PAR64	AA10	S_PAR64		
R23	S_PCIXCAP	R23	S_PCIXCAP		
AB17	S_PERR#	AB17	S_PERR#		
AA23	S_REQ1GNT#	AA23	S_REQ0#		
AA2	S_REQ2#	AA2	S_REQ1#		
W2	S_REQ3#	W2	S_REQ2#		
AB3	S_REQ4#	AB3	S_REQ3#		
AB5	S_REQ5#	AB5	S_REQ4#		
AC3	S_REQ6#	AC3	S_REQ5#		
AB13	S_REQ64#	AB13	S_REQ64#		

U23	S_RST#	U23	S_RST#		
AB19	S_SERR#	AB19	S_SERR#		
AB20	S_STOP#	AB20	S_STOP#		
Y14	S_TRDY#	Y14	S_TRDY#		
AB21	S_VDDA	AB21	S_VCCA		
T1	VDD2	T1	S_VIO		
F21	JTG_TCK	F21	TCK		
C22	JTG_TDI	C22	TDI		
B23	JTG_TDO	B23	TDO		
D22	JTG_TMS	D22	TMS		
C23	JTG_TRST#	C23	TRST#		
D11	VDD	D11	VCC		
D13	VDD	D13	VCC		
D15	VDD	D15	VCC		
D9	VDD	D9	VCC		
J20	VDD	J20	VCC		
J4	VDD	J4	VCC		
L20	VDD	L20	VCC		
L4	VDD	L4	VCC		
N20	VDD	N20	VCC		
N4	VDD	N4	VCC		
R20	VDD	R20	VCC		
R4	VDD	R4	VCC		
Y11	VDD	Y11	VCC		
Y13	VDD	Y13	VCC		
Y15	VDD	Y15	VCC		
Y9	VDD	Y9	VCC		
A12	VDD2	A12	VCCP		
A22	VDD2	A22	VCCP		
A8	VDD2	A8	VCCP		
AC12	VDD2	AC12	VCCP		
AC16	VDD2	AC16	VCCP		
AC2	VDD2	AC2	VCCP		
C5	VDD2	C5	VCCP		
D17	VDD2	D17	VCCP		
D19	VDD2	D19	VCCP		
D5	VDD2	D5	VCCP		
D7	VDD2	D7	VCCP		
E20	VDD2	E20	VCCP		
E4	VDD2	E4	VCCP		
G20	VDD2	G20	VCCP		
G4	VDD2	G4	VCCP		
M1	VDD2	M1	VCCP		
U20	VDD2	U20	VCCP		
U4	VDD2	U4	VCCP		
W20	VDD2	W20	VCCP		
W4	VDD2	W4	VCCP		

Y17	VDD2	Y17	VCCP
Y19	VDD2	Y19	VCCP
Y5	VDD2	Y5	VCCP
Y7	VDD2	Y7	VCCP
A1	GND	A1	VSS
A10	GND	A10	VSS
A11	GND	A11	VSS
A14	GND	A14	VSS
A18	GND	A18	VSS
A23	GND	A23	VSS
A6	GND	A6	VSS
AA21	GND	AA21	VSS
AA3	GND	AA3	VSS
AB2	GND	AB2	VSS
AB22	GND	AB22	VSS
AC1	GND	AC1	VSS
AC10	GND	AC10	VSS
AC13	GND	AC13	VSS
AC14	GND	AC14	VSS
AC18	GND	AC18	VSS
AC23	GND	AC23	VSS
AC6	GND	AC6	VSS
B2	GND	B2	VSS
B22	GND	B22	VSS
C21	GND	C21	VSS
C3	GND	C3	VSS
D12	GND	D12	VSS
D16	GND	D16	VSS
D20	GND	D20	VSS
D4	GND	D4	VSS
D8	GND	D8	VSS
F1	GND	F1	VSS
F23	GND	F23	VSS
H20	GND	H20	VSS
H4	GND	H4	VSS
K1	GND	K1	VSS
K23	GND	K23	VSS
L23	GND	L23	VSS
M20	GND	M20	VSS
M4	GND	M4	VSS
N1	GND	N1	VSS
P1	GND	P1	VSS
P23	GND	P23	VSS
T20	GND	T20	VSS
T4	GND	T4	VSS
V1	GND	V1	VSS
V23	GND	V23	VSS

Y12	GND	Y12	VSS	
Y16	GND	Y16	VSS	
Y20	GND	Y20	VSS	
Y4	GND	Y4	VSS	
Y8	GND	Y8	VSS	